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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,107	01/20/2004	Leonard Forbes	M4065.0492/P492-A	6955

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DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street, NW
Washington, DC 20037

EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,107	FORBES ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-31* is/are allowed.

6)☒ Claim(s) *32-34 and 37* is/are rejected.

7)☒ Claim(s) *35 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/20/04, 02/08/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/759,107, which is a divisional of Application Serial No. 10/164,611 filed on 10 June 2002, now US Patent No. 6,900,521.

2. The preliminary amendment filed on 20 January 2004 canceled claims 1-19. Accordingly, claims 20-37 currently pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kencke et al. (US 6,313,487 B1) in view of Fitzgerald (US 202/0123167 A1).[1]

The Kencke et al. patent (Kencke) discloses a method of forming a transistor structure (fig. 3 and col. 3, lines 20-54). The method comprises: providing at least one silicon germanium vertical pillar extending outwardly from a surface of a semiconductor substrate 10 (fig. 3 and col. 3, lines 22-31), the silicon germanium vertical pillar comprising a first source/drain layer 12 formed over the semiconductor substrate (col. 3, lines 22-31), a silicon

germanium layer 24 formed over the first source/drain layer (col. 3, lines 22-31), and a second source/drain layer 14 formed over the relaxed silicon germanium layer (col. 3, lines 22-31); and forming a strained silicon layer 30 in contact with the at least one silicon germanium vertical pillar (fig. 3 and col. 3, lines 39-48).

While Kencke discloses a silicon germanium layer formed over a first source/drain layer, Kencke does not disclose forming a relaxed silicon germanium layer over the first source/drain layer. Instead, the silicon germanium layer is preferably a compressively strained silicon germanium layer (col. 3, lines 36-39). The Fitzgerald pre-grant published application (Fitzgerald), on the contrary, discloses forming a relaxed silicon germanium layer (figs. 7A-7D and accompanying text). The method comprises forming a relaxed silicon germanium layer 700 (fig. 7A and par. par. 37, lines 5-7), and forming a strained silicon layer 702 on the surface thereof (fig. 7A and par. par. 37, lines 5-7).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Kencke by forming a relaxed silicon germanium layer, as taught by Fitzgerald, because the relaxed silicon germanium layer creates tension in the subsequently formed silicon layer and, thereby, increases carrier mobility (Fitzgerald - par. 4, lines 6-13). An increase

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[1] Applicant submitted the Kencke et al. patent as prior art.

in carrier mobility results in an increase in the frequency of operation of the MOS transistor and the associated circuitry (Fitzgerald - par. 4, lines 6-13).

4. Claims 33 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kencke in view of Fitzgerald as applied to claim 32 above, and further in view of Comfort et al. (US 5,308,785).

Kencke discloses growing each of the silicon germanium layer and the silicon layer using an epitaxial growth process (col. 3, lines 22-31). While Kencke discloses using an epitaxially growth process, Kencke does not explicitly teach that the silicon germanium and silicon layers are epitaxially grown using an ultra high vacuum chemical vapor deposition (UHVCVD) process. However, the Comfort et al. patent (Comfort) discloses forming a silicon germanium layer 20 and a silicon layer 30 using a UHVCVD process. Comfort discloses a semiconductor fabrication process, which comprises epitaxially growing a silicon germanium layer 20 and a silicon layer 30 using a UHVCVD process (fig. 2; col. 3, line 67 - col. 4, line 3; and col. 4, lines 19-25). According to Comfort, one advantage of using a UHVCVD epitaxially growth process is the process does not require an in-situ cleaning (col. 4, lines 6-8).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the combination of Kencke and Fitzgerald by epitaxially growing the silicon germanium and silicon layers of Kencke using a

UHVCVD process, as taught by Comfort, because UHVCVD processes do not require an in situ cleaning.

5. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Kencke in view of Comfort as applied to claim 33 above, and further in view of Wolf et al. ("Silicon Epitaxial Growth," Silicon Processing for the VLSI Era - Vol. 1: Process Technology).

In Comfort, the process for growing the silicon germanium layer comprises using germane as the germanium source gas and silane as the silicon source gas (col. 4, lines 3-6). Comfort does not teach the use of dichlorosilane as the silicon source gas. However, the Wolf et al. (Wolf) non-patent literature reference teaches that silane and dichlorosilane are art-recognized equivalent source gases for silicon in epitaxial deposition (page 133 - first paragraph, lines 1-3).

Therefore, since silane and dichlorosilane are art-recognized equivalent silicon source gases used for epitaxial deposition, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to use dichlorosilane as the silicon source gas, in place of silane, in the UHVCVD process for forming the silicon germanium layer.

Allowable Subject Matter

6. Claims 20-31 are allowable over the prior art of record. The prior art of record does not anticipate, teach or suggest a method of forming a transistor substantially as claimed, wherein the method comprises forming a strained silicon layer on each sidewall of the pillar.

7. Claims 35 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
18 June 2005

Mary Wilczewski
Primary Examiner